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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/028,850	12/20/2001	Eric J. Hansen	Hansen 1-1	3337

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EXAMINER	
WONG, LINDA	
ART UNIT	PAPER NUMBER
2634	

DATE MAILED: 08/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/028,850	HANSEN ET AL.	
	Examiner	Art Unit	
	Linda Wong	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see Applicant Arguments, filed 6/13/2005, with respect to the rejection(s)of claim(s) 1-12, under Perrott et al in view of Savelli have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Trichet et al (US Patent No.: 6211747).

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. **Claims 2 and 13** are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claims 2 and 13 recites "the first and second data-modulated input signals have substantially complementary frequency responses" which is not supported in the specification. A definition or description is necessary to understand the terminology.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-6 and 13-14** are rejected under 35 U.S.C. 102(b) as being anticipated by Trichet et al (US Patent No.: 6211747).

   a. **Claim 1**, Trichet et al discloses a frequency synthesizer comprising a phase locked loop (PLL) (Fig. 1, labels 30,40,10,20), a first data modulated path configured to generate a first modulated signal based on the input signal (Fig. 1, labels 90,60,70,41 and 10) and applying such the first modulated signal to a voltage controlled oscillator (VCO) (Fig. 1, label 141) and generating a second modulated signal (Fig. 1, labels 90,60,61,161,20) and providing the second data modulated signal to a frequency divider to control the division factor (Fig. 1, label 121).

   b. **Claim 2**, Trichet et al discloses a frequency synthesizer comprising a first and second data modulated signal wherein these signals have complementary transfer characteristics. (Col. 2, lines 8-12)

   c. **Claim 3**, Trichet et al discloses a PLL comprising a phase detector (Fig. 1, label 30), a low pass loop filter (Fig. 1, label 40, Col. 5, lines 67 and Col. 6, line 1), a VCO connected to the filter (Fig. 1, label 10) and a frequency divider (Fig. 1, label 20) and feedback from the divider to the phase detector (Fig. 1, label 120).

   d. **Claim 4**, Trichet et al discloses an in-band and out-of-band modulation, wherein the in-band modulation effects the division factor of the divider produces frequency response that does not exceed the low pass filter and the out-of-band

modulation effects the VCO produces a frequency response output from the VCO that exceeds the low-pass filter or a high pass frequency response. (Col. 1, lines 60-67, Col. 2, lines 1-5, and lines 13-22, and Col. 3, lines 45-48 and lines 49-52)

e. **Claim 5**, Trichet et al discloses a phase detector (Fig. 1, label 30) generating a phase difference signal (Fig. 1, label 130) based on the reference signal (Fig. 1, label 150) and the frequency divider output (Fig. 1, label 120), a loop filter (Fig. 1, label 40, Col. 5, lines 67 and Col. 6, line 1), a VCO outputting modulated signal (Fig. 1, label 110) based on the loop filter (Fig. 1, label 40) and the first modulated signal (Fig. 1, labels 60,70,41,10) and a frequency divider (Fig. 1, label 20) configured to divide the signal based on the data modulated output signals from the VCO (Fig. 1, label 110) and the second modulated signal (Fig. 1, labels 90,61,21, and 60), wherein the second modulated signal determines the division factor (Col. 3, lines 25-34 and Abstract, lines 11-12).

f. **Claim 6**, Trichet et al discloses a sigma-delta modulator for generating a modulated signal, which controls the N factor or divider modulus of the frequency divider (Fig. 1, label 121, Col. 3, lines 25-34 and Abstract, lines 11-12).

g. **Claim 13** inherits all the limitations of claims 1 and 2.

h. **Claim 14** inherits all the limitations of claims 1 and 4.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 7-11, and 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Trichet et al (US Patent No.: 6211747) in view of Perrott et al (US Patent No.: 6008703).

   a. **Claim 7**, Although Trichet et al fails to teach scaling block for adjusting the gain and carrier selection block for the second modulation signal, Perrott et al discloses a digital compensation and transmit filtering component, wherein the transfer function response is related to adjusting the gain or amplitude and the bandwidth and a carrier signal insertion. (Fig. 2A, labels 46, 54 and 52, Abstract, lines 5-23, Col. 7, lines 55-62 and Col. 7, lines 63-67 and Col. 8, line 1) It would be obvious to one skilled in the art to include a digital compensation and transmit filtering to connect to the carrier insertion block (Fig. 1, label 61) disclosed in Trichet et al's invention to overcome strict bandwidth limits, large power consumption and amplifying undesired noise while allowing indirect or inband modulation. (Col. 2, lines 19-35 and lines 55-67, Col. 3, lines 1-6 and Col. 3, lines 30-43)

   a. **Claim 8**, Perrott et al discloses a Guassian frequency shifted keyed modulation and the input data signal is Gaussian low-pass filtered (Fig. 2A, label 46) prior

to the first modulation path. Although Perrott et al does not disclose a second modulation path, Jorgensen discloses a second modulation path filtered by a Guassian filter (Fig. 1, label 9). It would be obvious to one skilled in the art to add a second data-modulation path to Perrott et al's invention to generate modulated output with a frequency within the PLL bandwidth.

b. **Claim 9**, Perrott et al discloses a sigma-delta modulator quantizes noise or spurious signals to high frequencies, which are attenuated by the PLL. (Col. 8, lines 7-14 and lines 39-54)

b. **Claim 10**, Perrott et al discloses a sigma-delta modulator comprised of an adder (Fig. 8A and 8B, Col. 16, lines 27-38) and a noise-shaping loop (Fig. 8B, Col. 16, lines 27-38), wherein the adder generates a summation signal bases on the input data signal and an output from the noise-shaping loop (Fig. 8A and 8B). A set of most significant bits are generated by adding the loop input and used to adjust the divider factor in the PLL (Col. 16, lines 27-53) and a set of least significant bits are generated from the previous clock accumulation and fed back (Fig. 8B, label error and feedback to adder and Col. 16, lines 27-53)

c. **Claim 11**, Perrott et al discloses a sigma-delta modulation, which inherently functions as a quantizer wherein the error is fed back to the accumulator or quantizer. (Fig. 8A and 8B)

d. **Claim 15** inherits all the limitations of claims 1 and 10.

e. **Claim 16** inherits all the limitations of claim 11.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

   a. Mutz (US Patent No.: 5130676)

   b. Taromaru et al (US Patent No.: 5281930)

   c. Gilling (US Patent No.: 5604468)

   d. Matsuura (US Patent No.: 4528522)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linda Wong whose telephone number is 571-272-6044. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Chin can be reached on (571) 272-3056. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Linda Wong

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